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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chih-Tsung Lin

Serial No.: 10/800,175

Filed: March 12, 2004

For: Knowledge Slicing and
Encapsulating Method in a
Semiconductor Manufacturing System

Attorney Docket No.:
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Examiner: Hirl, Joseph P.

Art Unit: 2129

Conf. No.: 8620

Commissioner for Patents
Mail Stop Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.131

I, Chih-Tsung Lin, being duly sworn, depose and say:

1. That I am the inventor for the above-identified Patent Application;
2. That I have reviewed the claims of this Application;
3. That I conceived in Taiwan (Republic of China), a member of the World Trade

Organization, prior to June 5, 2003, the effective date of the cited United States Pub. No. 2004/0249829, the invention as set forth in the above-captioned application, and in particular, a method for managing semiconductor manufacturing knowledge that includes defining a hierarchy of interests in the semiconductor knowledge with data targets and results, storing the hierarchy of interest, developing a connectivity relationship diagram to reflect the dependency between the data targets and the results, implementing the connectivity relationship diagram, coupling the implemented connectivity relationship diagram with the stored hierarchy of interest, identifying at least one data source for the data targets, and coupling the implemented connectivity relationship diagram to the at least one data source.

4. That I conceived in Taiwan (Republic of China), a member of the World Trade Organization, prior to June 5, 2003, the effective date of the cited United States Pub. No. 2004/0249829, the invention as set forth in the above-captioned application, and in particular, a method for managing semiconductor manufacturing knowledge that includes defining a hierarchy of interests in the semiconductor knowledge with data targets and results, storing the hierarchy of interest, developing a dynamic master logic diagram to reflect the dependency between the data targets and the results, implementing the dynamic master logic diagram, coupling the dynamic master logic diagram with the

stored hierarchy of interest, identifying at least one data source for the data targets, and coupling the dynamic master logic diagram to the at least one data source.

5. That I conceived in Taiwan (Republic of China), a member of the World Trade Organization, prior to June 5, 2003, the effective date of the cited United States Pub. No. 2004/0249829, the invention as set forth in the above-captioned application, and in particular, a semiconductor manufacturing knowledge management system that includes at least one data source, a conceptual layer stored in a storage unit, and a logic layer coupled to the conceptual layer and at least one data source.

6. Attached as Exhibited A is a copy of my "TSMC Invention Disclosure" that was prepared and provided to my employer prior to June 5, 2003 evidencing conception of the above-captioned invention.

7. That from before June 5, 2003 to March 12, 2004, the filing date of U.S. Ser. No. 10/800,175, I diligently worked toward reducing the claimed invention to practice and worked with patent counsel in the preparation of a patent application for the claimed invention. At no time did we abandon, suppress, or conceal the invention claimed in the above-captioned application.

That the statements made herein is of our my knowledge and are true and made on information and belief that are believed to be true.

I acknowledge that any willful false statements and the like made herein are punishable by fine or imprisonment, or both, and may jeopardize the validity of the application or any patent issuing thereon.

Chih-Tsung Lin
Chih-Tsung Lin

Dated: 2006/11/29



TSMC INVENTION DISCLOSURE

SECURITY B
TSMC-RESTRICTED
D

CTLINE/TSMC on

Status : 智財處處理完成

Current Processor : 011672 : 林志聰

| Disclosure No. | Received date | | Process priority | | | |
|---|-------------------------------|---------|------------------|------------|----------|--------------------|
| Emp. No. | Full name of inventor(s) | | Dept. | Dept. Code | Ext. No. | E-mail Address |
| for inventors from outside of tsmc, please use "X66" instead. | English, the same as passport | Chinese | | | | |
| 011672 | Chih-Tsung Lin | 林志聰 | SDEV | 3026 | 7072786 | CTLINE@tsmc.com.tw |
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EXHIBIT
A
PENGAD 800-631-6989

- Title of invention - (English only)
A Knowledge Slicing and Encapsulating Method in Expert System
- Related disclosure(s) -
- Assignee - 本發明屬於1.TSMC 或 2.由TSMC與其他公司共同擁有
☒ 1. TSMC ☐ 2. TSMC &
- Laboratory Notebook / 研究紀錄簿相關資訊
This idea was shown on page of the laboratory notebook with serial number of (such as 2002-00036).
Please attach a copy of the related pages.
- Invention related information / 本發明相關資訊 -
 - Will this invention be disclosed, published, utilized, commercialized or implemented in Customer's product(s)?
☒ No. ☐ Yes. When (ex. 03/31/2003) 請務必填寫本發明之預定論文發表或展覽或販賣或實施於客戶產品的日期, 以加速申請流程.
 - Other special request :

- Classification – (Multiple choices are possible / 以下 1 至 4 項可多選)

1. Where will the invention be used / 本發明的潛在使用者：

- ☒ (Others) Company who builds expert system may use this method to
☒ At TSMC
☐ Unknown
☐ Probably will not be used
☐ Used by most IC companies
model domain knowledges

2. Technology generation / 本發明適用於 (應用於一般技術請選擇 General, 0.25um 以上或 65nm 以下請選擇 others)：

- ☒ General ☐ 0.18um ☐ 0.13um ☐ 65nm ☐ Unknown
☐ 0.25um ☐ 0.15um ☐ 90nm ☐ Others

3. Technology / 本發明應用在 (應用於一般技術請選擇 General, 無法歸類請選擇 others)：

- ☒ All Technology ☐ Image sensor ☐ Mixed-Signal/RF ☐ SiGe
☐ DRAM ☐ Logic ☐ MRAM ☐ SRAM
☐ Embedded ☐ MEMS ☐ NVM ☐ Others

4. Field of invention / 本發明的技術領域 (若無法歸類, 請選擇 Others)：

- | | | | |
|--|---|--|--|
| <input type="checkbox"/> Device | <input type="checkbox"/> Equipment/Litho/Mask | <input type="checkbox"/> Module/Diffusion | <input checked="" type="checkbox"/> Software |
| <input type="checkbox"/> Business method | <input type="checkbox"/> Equipment/Thin Film | <input type="checkbox"/> Module/Etch | <input type="checkbox"/> Testing/QR |
| <input type="checkbox"/> Circuit design | <input type="checkbox"/> Integration | <input type="checkbox"/> Module/Litho/Mask | <input type="checkbox"/> Others |
| <input type="checkbox"/> Equipment/CMP | <input type="checkbox"/> Manufacturing Technology | <input type="checkbox"/> Module/Thin Film | |
| <input type="checkbox"/> Equipment/Diffusion | <input type="checkbox"/> Module/CMP | <input type="checkbox"/> Package/Assembly | |

- References similar to the invention / 與本發明相關的論文及/或專利 - (Please search for related patents on USPTO website / www.uspto.gov)
 - keyword(s) used / 專利查詢所使用的關鍵字 : DMLD (Dynamic Master Logic Diagram)
 - Related patent number(s) / 相關的專利號碼 : US5914875
 - Related Non-Patent article(s) and/or product(s) / 其他相關的論文名稱或產品型號 : Evaluating system behavior through Dynamic Master Logic Diagram (DMLD) modeling
- Old method(s) or product(s) for performing the purpose of this invention / 目前方法簡介 (English only)

Traditionally, the domain knowledge of experts is distributed in IT systems. Experts and developers face a dilemma of large amount of pieces knowledge discovering. Knowledge have to be extracted from implementation code in IT systems, but domain experts are not capable of that. Domain expert convert his experience and knowledge to requirement document, and then IT engineers implement it to a system. The knowledge translates to design documents and sources codes, it's a black box for domain expert. Since knowledge evolution is a requisite process for expert system as decision inference and diagnosis result is unsatisfied. Thus the original development flow is not applicable for decision-making and problems diagnosing system.
- Problems or disadvantages faced by old method(s) or product(s) / 目前方法所面臨的問題及缺點 (English only)

The black box leads to the following problems

 - Fractal knowledge is distributed in IT systems.
 - IT systems is a knowledge black box for domain experts
 - Difficulty to accumulate expert knowledge.
- General purpose of this invention / 發明目的 (English only) -

This invention proposes a method of knowledge encapsulating by applying layer design, it provides the excellent readability of knowledge representation and an integrated view to navigate pieces of knowledge.
- Advantages of this invention / 本發明的好處或優點 (English only)
 - To abstract knowledge and encapsulate it into conceptual/design/implementation layers for improving readability and reusability. It also provides a team development mechanism for different roles.
 - To integrate conceptual/design/implementation layers into a hierarchical view for knowledge digging.
 - To connect pieces of knowledge using distributed DMLD for knowledge surfing.
 - To provide an excusable and traceable design for knowledge inference engine.

- Points of this invention thought to be novel, list by items. Please identify which elements/steps are must and which elements/steps are optional / 請逐項列舉為達成發明目的所使用的新方法或手段, 即, 本發明與目前方法的主要不同處, 並請指出必要及非必要元件 (English only)

1. A method to slice and encapsulate knowledge for improving readability and reusability in decision support and diagnosis system, the method comprising the steps of:

- (1) Slice the knowledge into different layers (conceptual/design/implementation) from different roles (domain expert/knowledge architect/developer).
- (2) Using DMLD (Dynamic Master Logic Diagram) to model knowledge.
- (3) Domain expert sketches the system relationship and weighting in conceptual layer.
- (4) Designer implements the inference flow and logic in design layer.
- (5) Developer defines connectivity gates as the pins of IC to connect another distributed DMLD or resources in implementation layer.

(6) Encapsulate these conceptual/design/implementation layers into an integrated hierarchical view

2. An integrated development environment of DMLD for claimed method, the environment comprising the mechanisms of:

- (1) Grouping presentation symbols into conceptual/design/implementation layers.
- (2) Encapsulating conceptual/design/implementation layers into an integrated hierarchical view.
- (3) A defined set of logic/computational for inference logic.
- (4) A defined set of connectivity gates for resources accessing and DMLD gates to connect distributed DMLD with a horizontal view.

Improvements:

After encapsulating 3 layer into a hierarchical view via IDE, inference engine parsing the knowledge by expanding conceptual, logical and implementation layer to a wide plane implementation layer. This invention providing the following improvements:

1. Sliced layers improve readability and reusability of denoted knowledge
 - a. Providing conceptual layer for expert to go knowledge surfing to extend knowledge width.
 - b. Integrating 3 layers into a hierarchical view for knowledge digging to extend knowledge depth
 - c. Using connectivity gates as IC pins to reuse pieces of knowledge for quickly assemble a new knowledge IC.
2. Provide a team development mechanism for different roles
3. Provide an excusable and traceable design for knowledge inference engine

- Detailed description of this invention / 發明的詳細敘述, 至少需包括一最好的實施例, 及/或其他適用於本發明的範例 (English only)

In contrast to system development process flow as showed in Fig.1, this invention proposed a knowledge slicing design to separate domain knowledge into 3 layers. They are conceptual layer, logic Layer, and implementation layer. (See Fig. 2) The first layer is conceptual layer, it represents for business knowledge from domain expert. The second layer is logic layer, it drills down from a node in conceptual layer to represent inference flow and logic. The third layer is implementation layer, it manages the IT knowledge for accessing the resource with codes inside. Different roles focus on different layers, all the design jobs are integrated in an unified developing environment. The IDE (Integrated Development Environment) encapsulates these denoted knowledge slicing in 3 layers into a hierarchical view just like an IC.

Conceptual layer:

This layer is adequate for business knowledge representation, the layout style similar to chess box , it stresses the goal and function/structure/behavior relationship. Each intersection node denotes there are connections between these two box. From conceptual layer, domain expert can easily model his knowledge in a widespread view, it also helps expert to analyze that if the current functions exists in company satisfied for some specific bussiness purpose.

Logic Layer:

This layer drills down from intersection node in conceptual layer. Logic layers composed of standard logic gates and intersection nodes with fuzzy degree. Fig.4 shows the sample of fuzzy clustering logic. The operation algorithm designed cooperatively in this layer by domain expert and knowledge architects. It provides a depth of expert's knowledge.

Implementation Layer:

This layer response for resource accessing, it acts as pins of IC. Due to resources exists with various kinds of forms, such as database, legacy application, another DMLD. For various forms of resource, the invention designs connectivity gates to access distributed resources. There are 3 gates defined as followed.

1. EAI gate, connect to legacy system using EAI products.
 2. DB gate, a subset of EAI gate, used to connect database resource with SQL statement inside.
 3. DMLD gate, connect to distributed DMLD exists in another inference engine.
- Resources accessing contain mass IT knowledge such as scripts, SQL codes, EAI scripts, these implemented by IT engineers. In another way, domain experts and knowledge architect unnecessarily realize these accessing techniques. All these detail hidden in this layer. But it is an executable foundation of a knowledge inference engine

- Other embodiments/methods/apparatus can be used to achieve the purpose of your invention by a potential infringer./其他可實施本發明目的的手段?或其他可迴避本發明的範例及做法?
None



- Attachments / 圖形請用附加檔 : Patent - A Knowledge Slicing and Encapsulating Method.doc

| | SIGNATURE OF WITNESS | DATE | SIGNATURE OF WITNESS | DATE |
|--|-------------------------|------|-------------------------|------|
| WITNESS: THE TWO WITNESSES WHOSE SIGNATURES APPEAR BELOW HAVE READ AND UNDERSTOOD THIS ENTIRE INVENTION DISCLOSURE. | | | | |

| DISCLOSURE SUBMITTED BY | | | |
|----------------------------|-----------------|-------------------------|------|
| INVENTORS' EMPNO | INVENTORS' NAME | INVENTOR'S SIGNATURE | DATE |
| 011672 | 林志聰 | | |

Processing Log :



A Knowledge Slicing and Encapsulating Method in Expert System

SDEV 林志聰

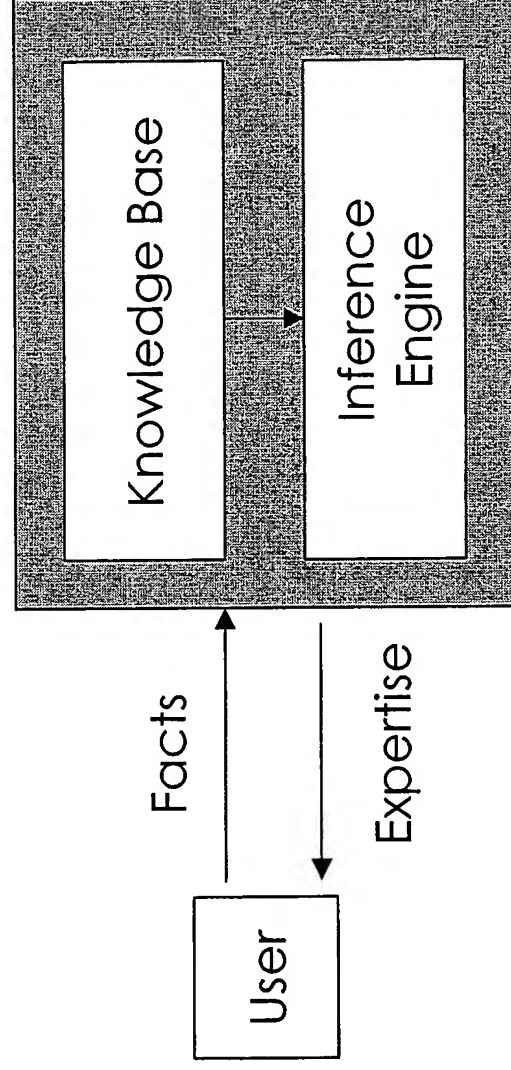
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Background Information (Expert System)

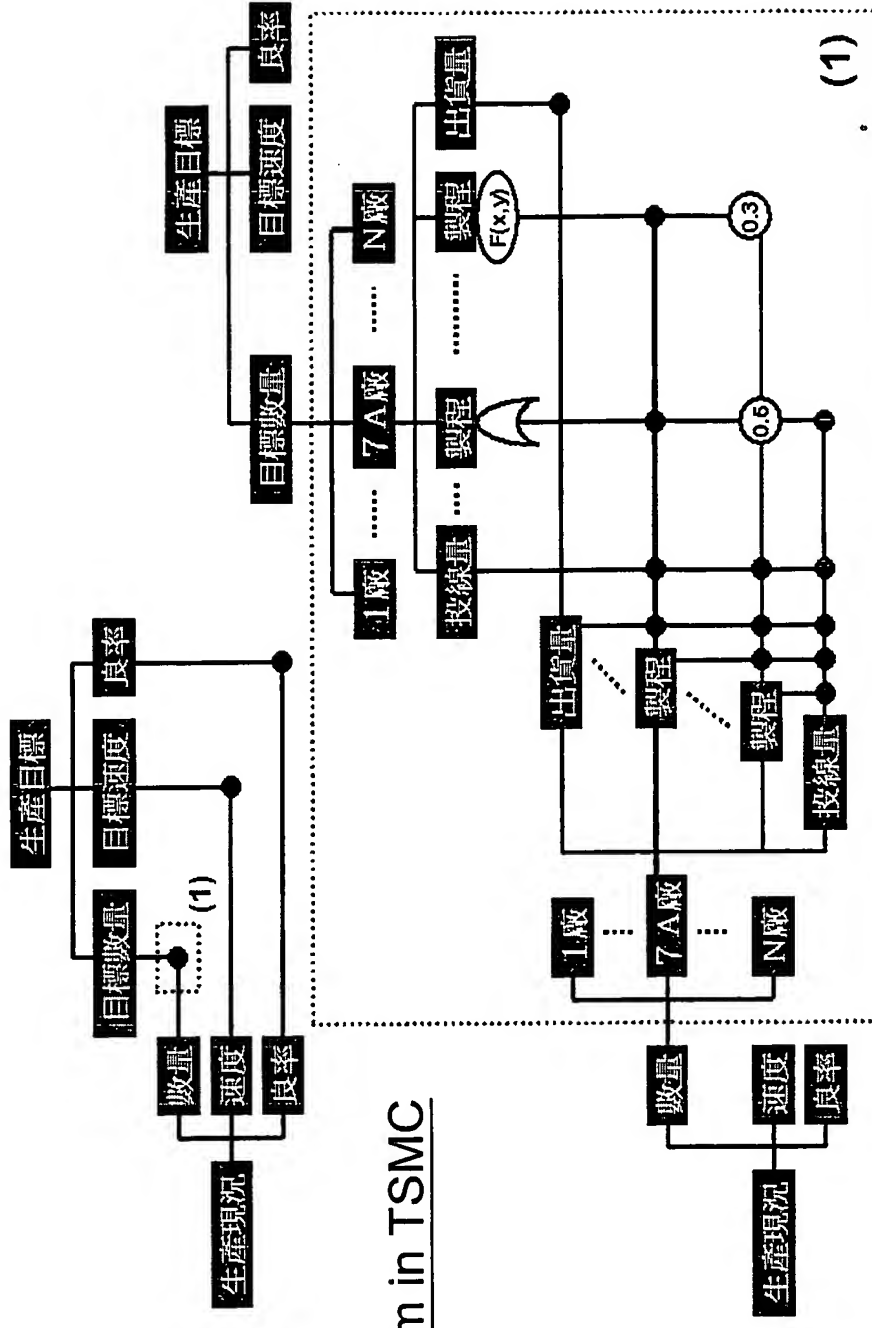


- Expert System

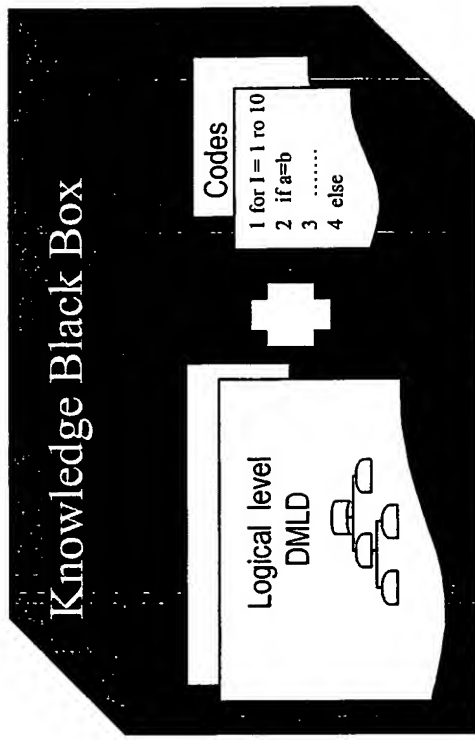
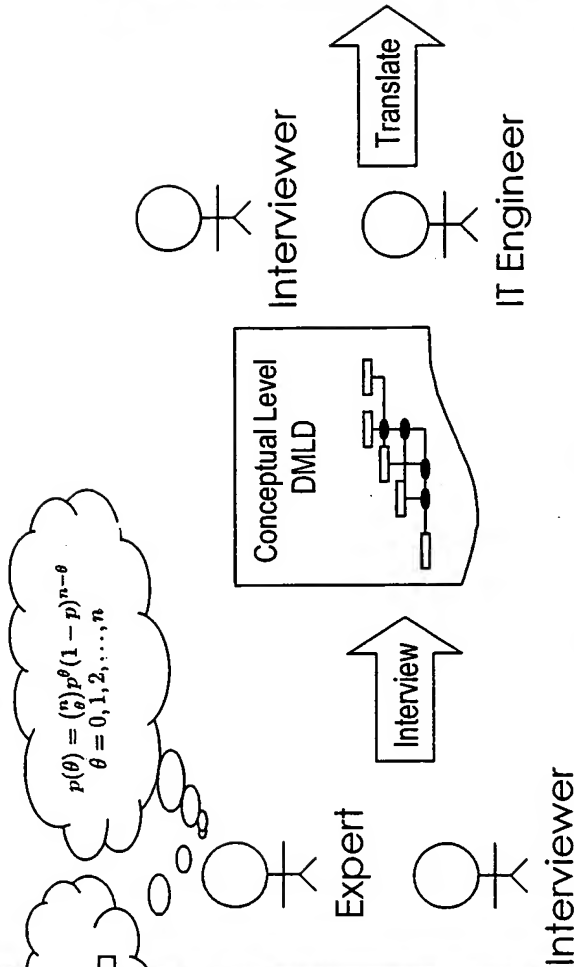
1. Decision making and problem diagnosing
2. Domain knowledge dominates the accuracy of inference result
3. Knowledge evolution is a requisite process



1. WAT
2. EQP
3. SPICE



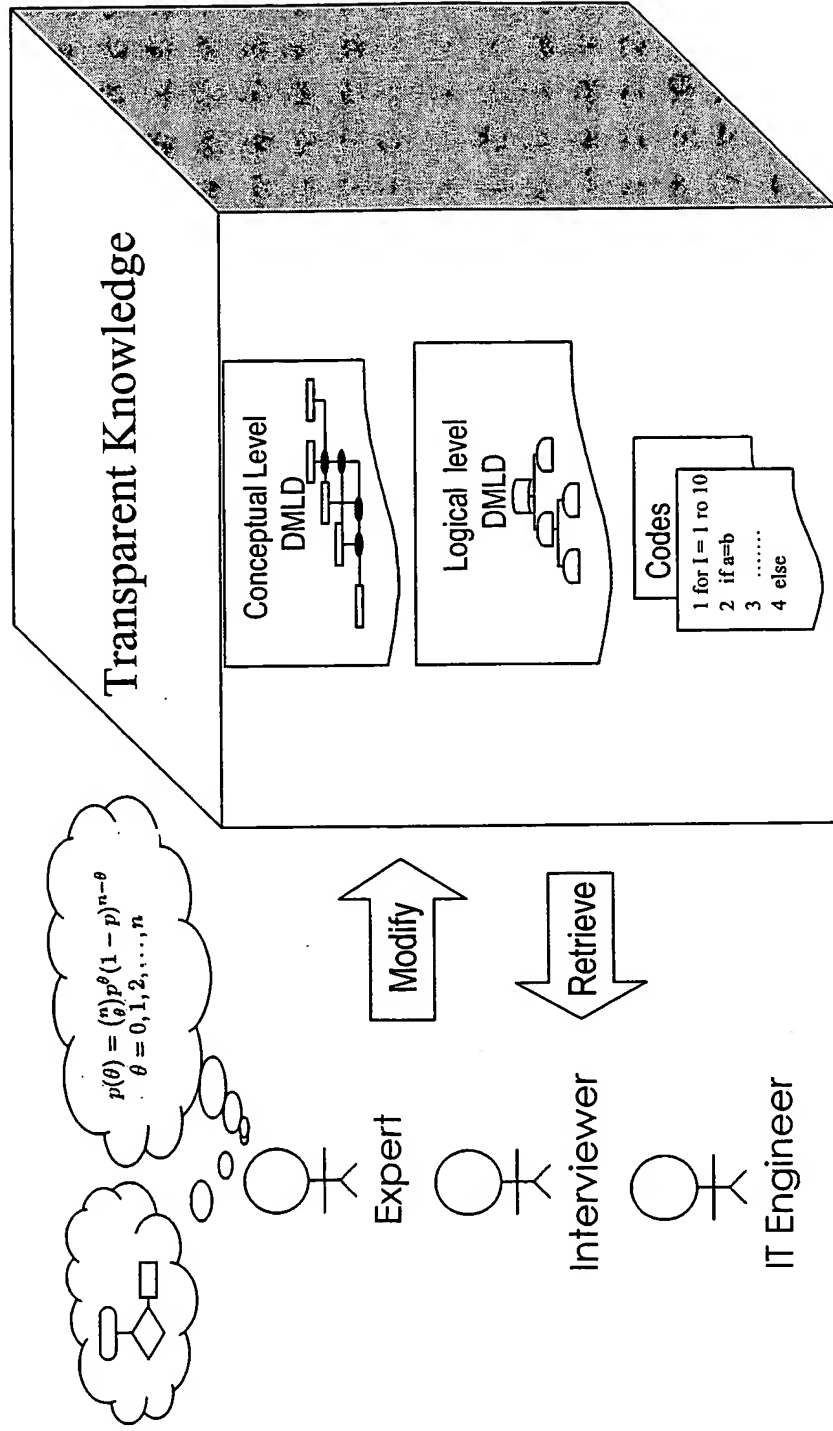
Background Information (Problem)



• Problems

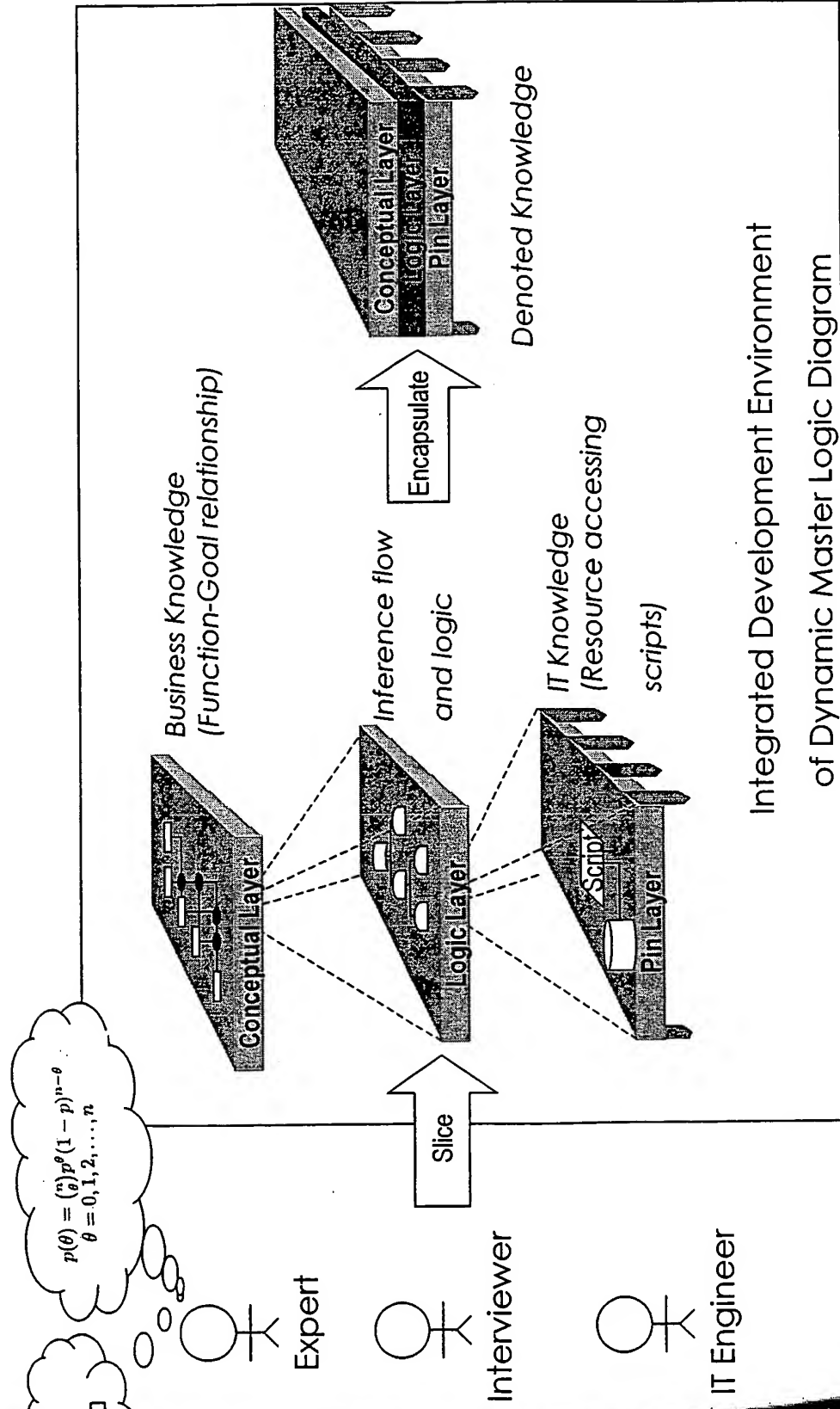
1. Knowledge mixed with Codes
2. IT systems is a knowledge black box for domain experts
3. Difficulty to accumulate expert knowledge.

Problem Solution



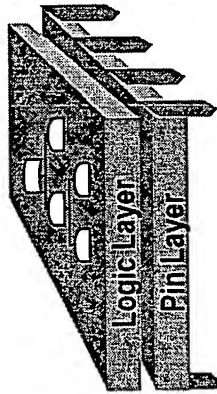
New Knowledge Development Process

Main Points of Claim



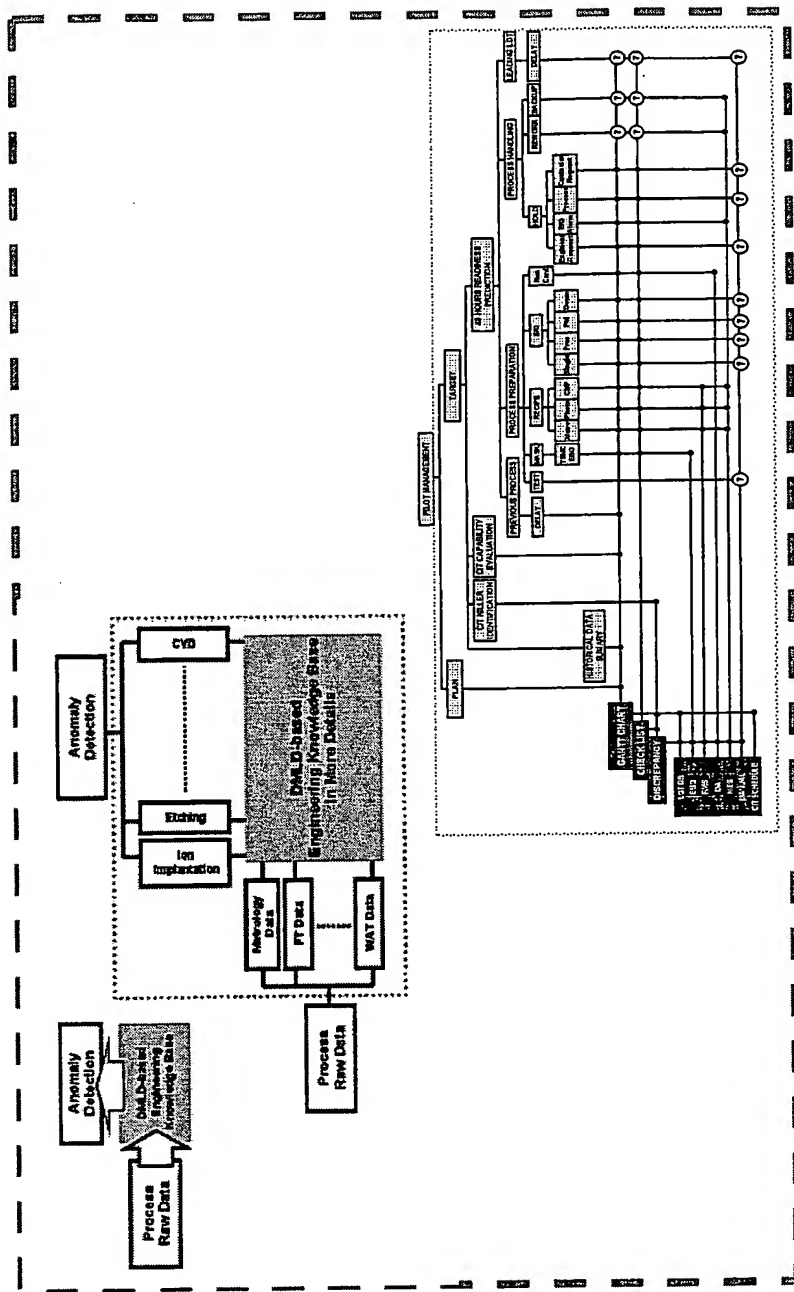


Business Knowledge
Function-Goal relationship)



Expert

Knowledge Slicing



Chess Box Layout (Function X Goal)

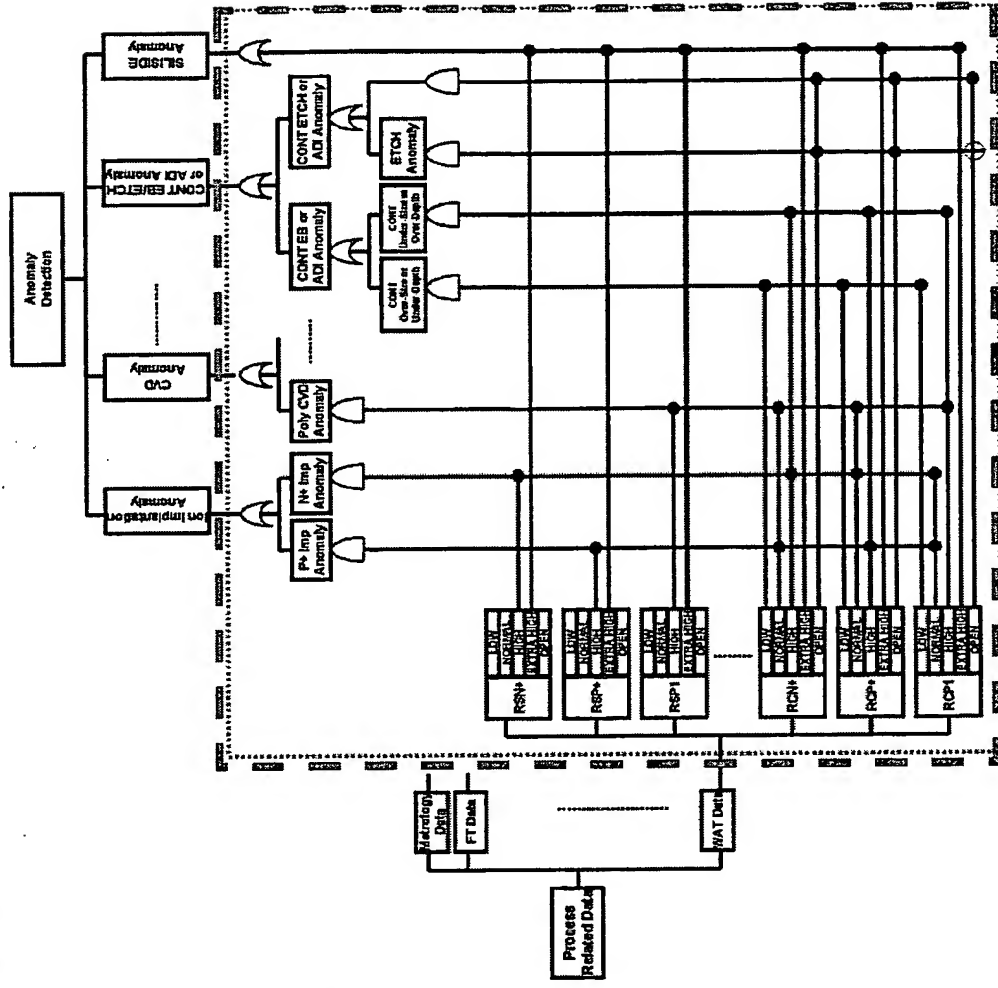
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Knowledge Slicing (cont.)



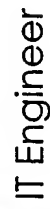
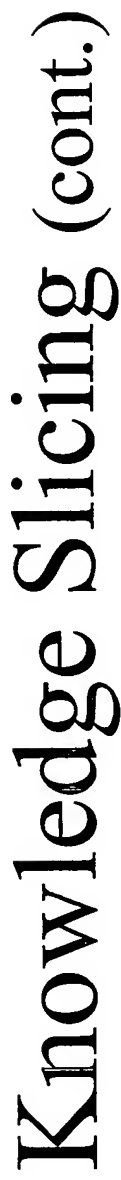
Expert

Interviewer

Logical Gate Layout (Fuzzy Logic)

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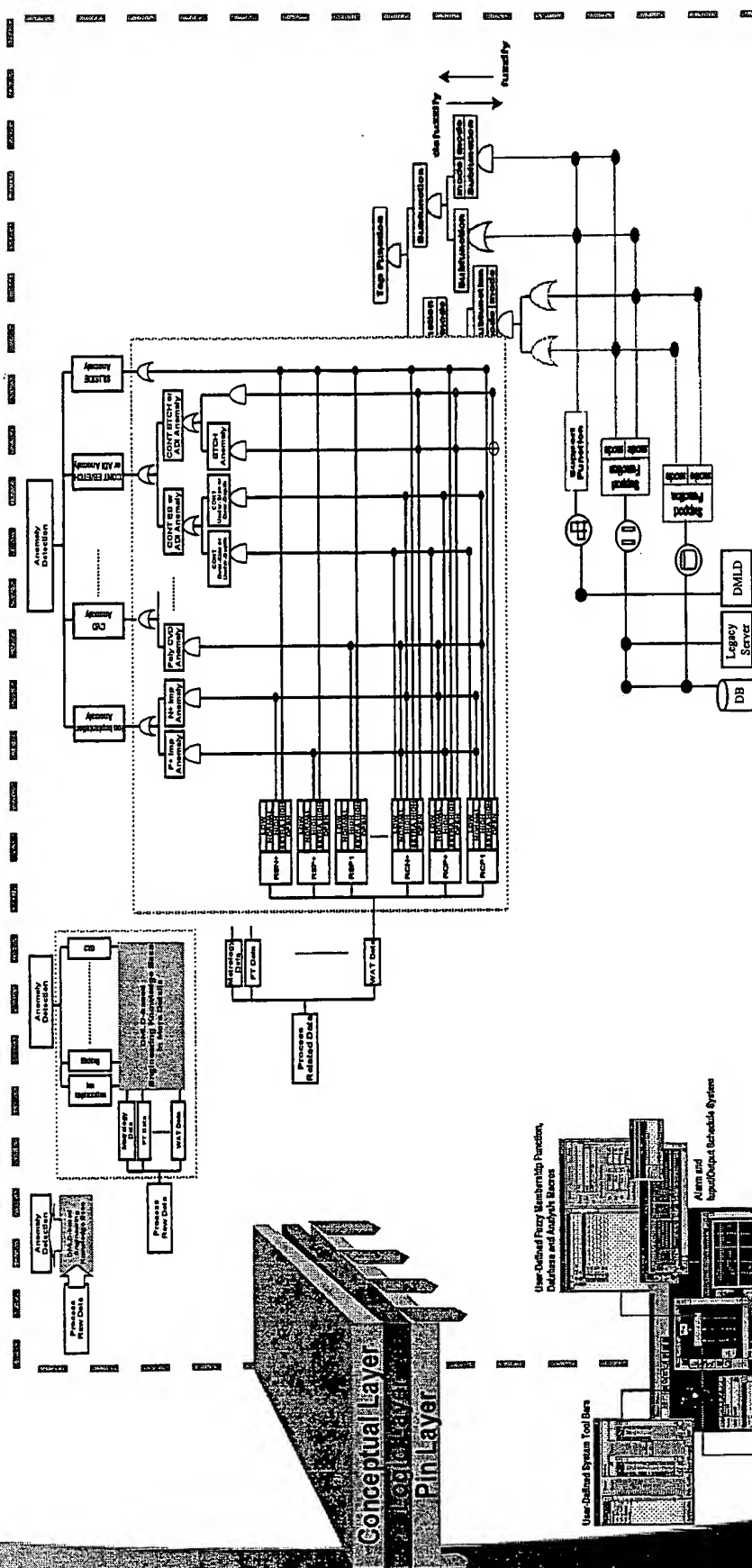


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Knowledge Encapsulating



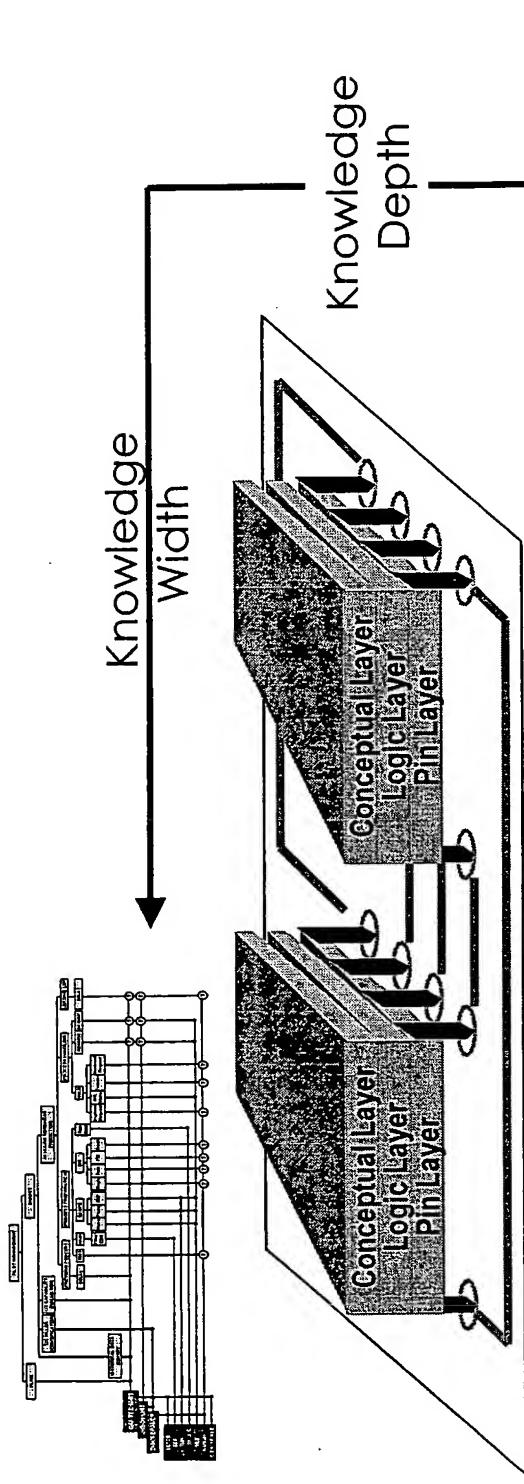
Integrated Development Environment of DMLD

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Improvements



- Sliced layers improve readability and reusability of denoted knowledge
 1. Providing conceptual layer for expert to go knowledge surfing.
 2. Integrating 3 layers into a hierarchical view for knowledge digging
 3. Using connectivity gates as IC pins to reuse pieces of knowledge
- Provide a team development mechanism for different roles
- Provide an excusable and traceable design for knowledge inference engine



Main Points of Claim

- **A method to slice knowledge for improving readability and reusability**
 - Slice the knowledge into different layers from different roles.
 - Domain expert sketches the system relationship and weighting in conceptual layer.
 - Designer implements the inference flow and logic in logical layer.
 - Developer write scripts in connectivity gates to connect another distributed DMLD or resources.
- **An integrated development environment of DMLD to encapsulate knowledge**
 - Encapsulating conceptual/logical/pin layers into an integrated hierarchical view.
 - A defined set of logic/computational for inference logic.
 - A defined set of connectivity gates for resources accessing and DMLD gates to connect distributed DMLD with a horizontal view.



Related Patent

- US5914875: Method and apparatus for diagnosing plant anomaly
- Provide a method for
 - diagnosing all abnormal events of a large-scaled complicated plant.
 - diagnosing anomalies of a plant with a user-friendly inference process.
- Reference

Yu-Shu Hu, et al., "Evaluating System Behavior Through Dynamic Master Logic Diagram (DMLD) Modeling," Proceedings of the Topical Meeting on Computer-Based Human Support Systems: Technology, Methods, and Future, Jun. 25, 1995, USA, pp. 218-224.
- Difference with my invention
 - US5914875 focus on knowledge inference method
 - My invention focus on knowledge notation method



Backup Slide

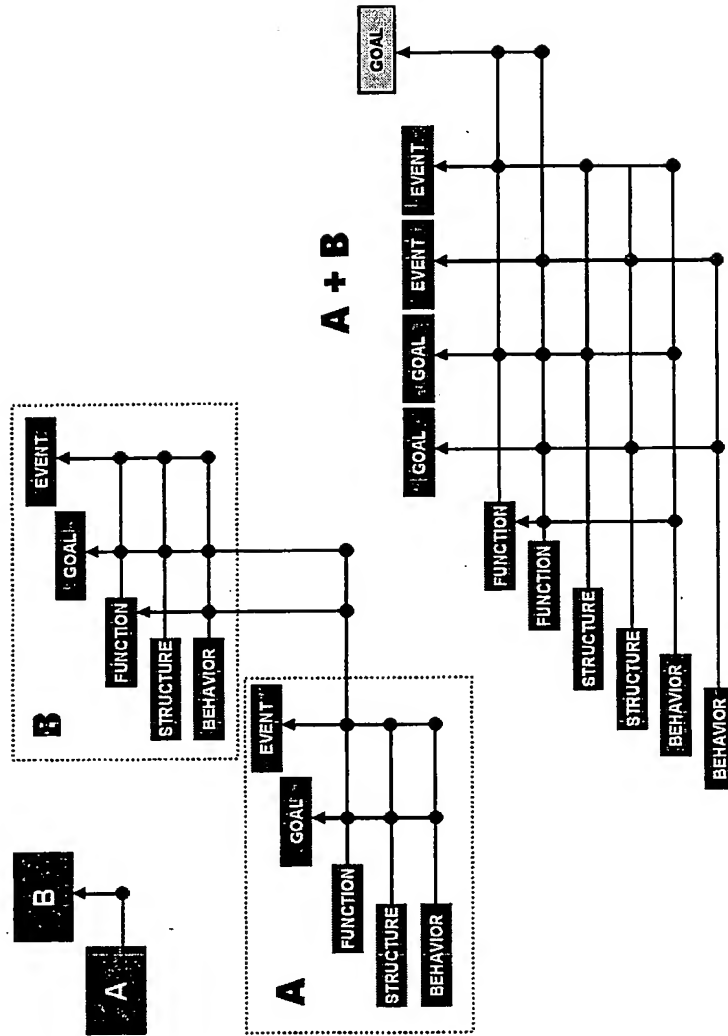
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Hierarchical Structure of DMIL



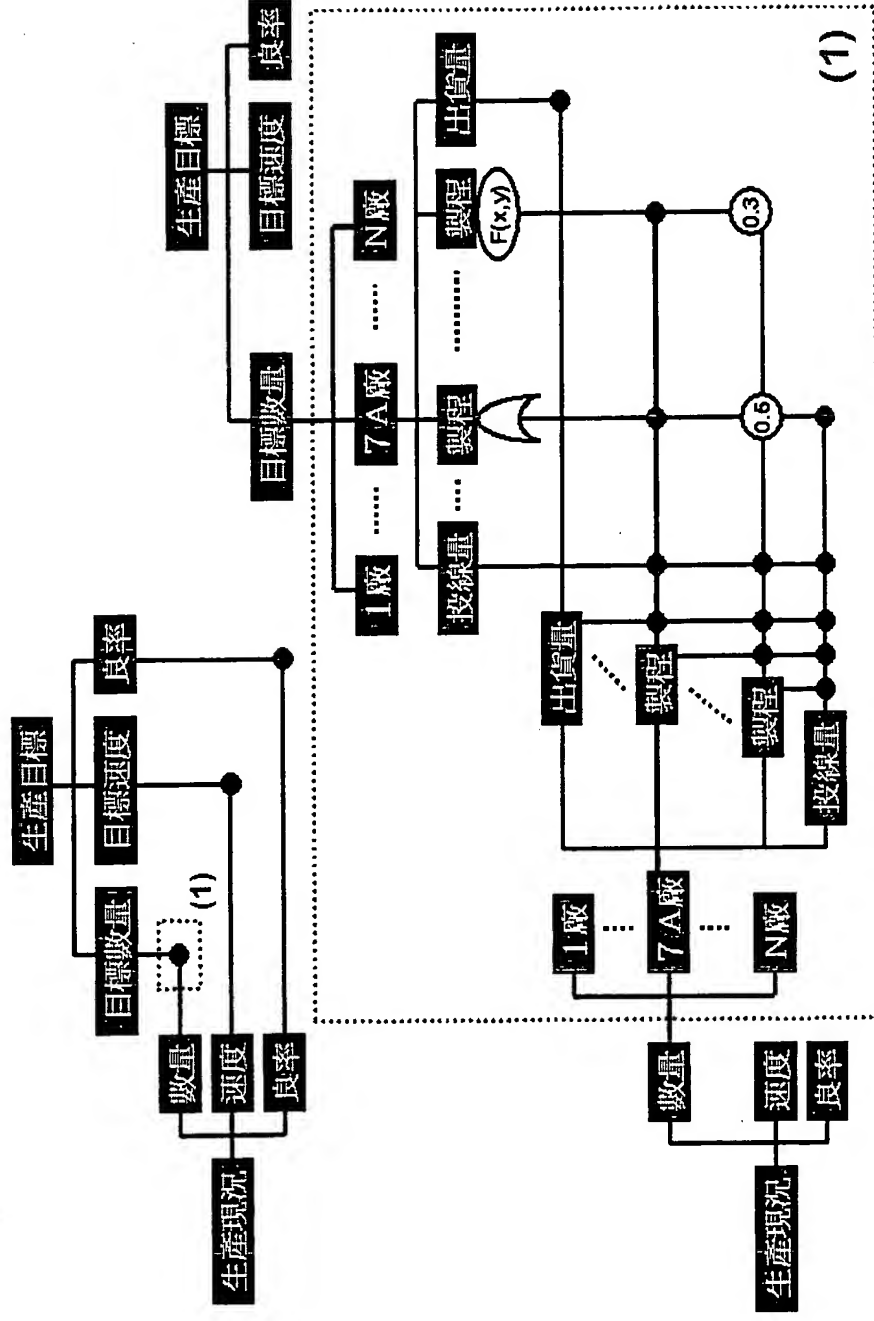


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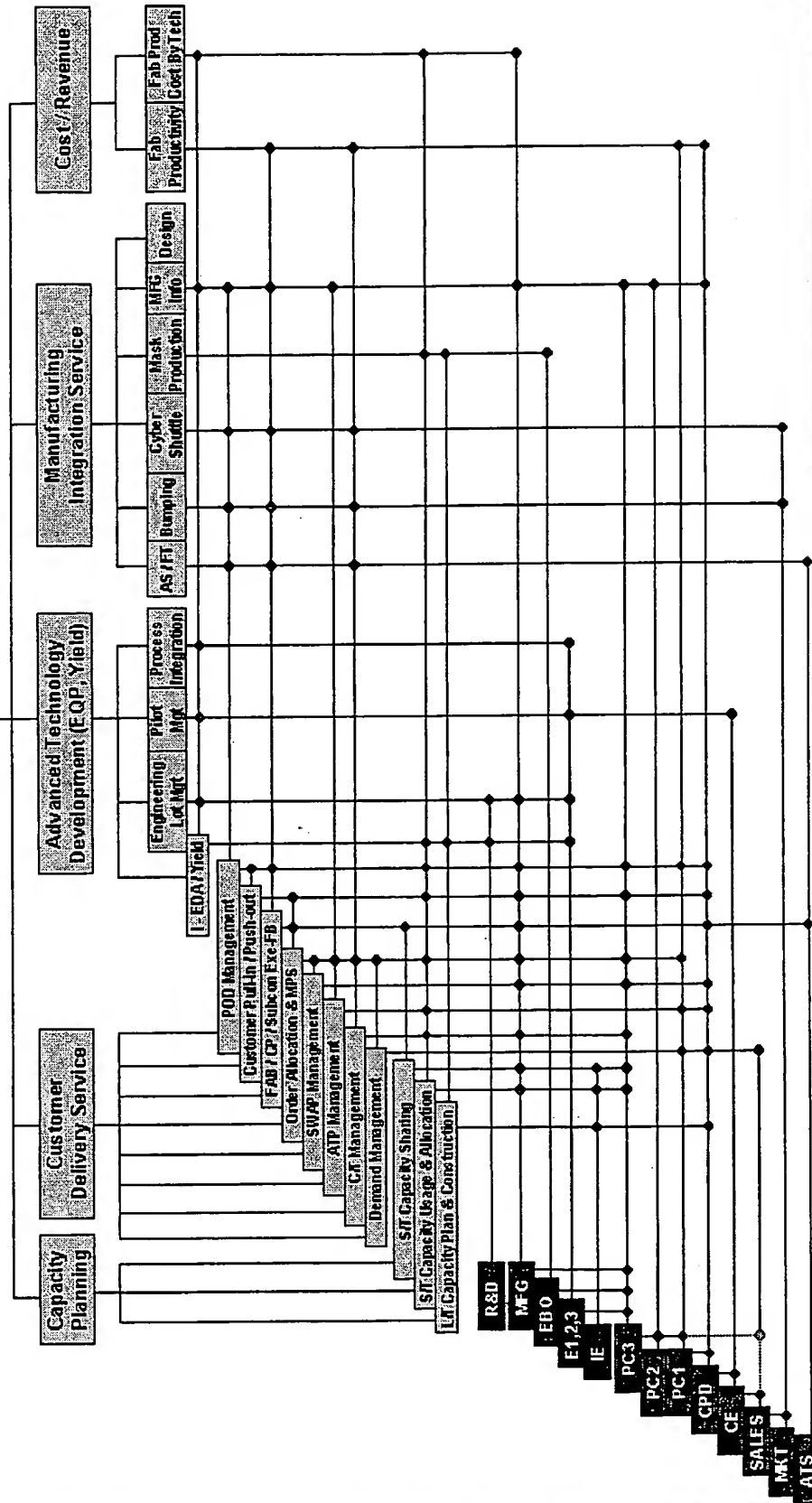
DMLD Example





Conceptual Layer Example

TSMC Enterprise
Manufacture Diagnostic and Digital Nervous System



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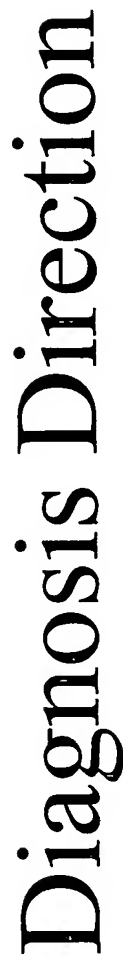
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